**Assignment Chapter 1:**

**Important Notes:**

* All the exercises are from the reference book.
* **Show your solution steps** so you receive partial credit for incorrect answers and I know you have understood the material. Don't just show us the final answer.

**Exercises.**

**1.1**[2] <§1.1> Aside from the smart cell phones used by a billion people, list and describe four other types of computers.

**1.2**[5] <§1.2> Th e eight great ideas in computer architecture are similar to ideas from other fields. Match the eight ideas from computer architecture, “Design for Moore’s Law”, “Use Abstraction to Simplify Design”, “Make the Common Case Fast”, “Performance via Parallelism”, “Performance via Pipelining”, Performance via Prediction”, “Hierarchy of Memories”, and “Dependability via Redundancy” to the following ideas from other fields:

1. Assembly lines in automobile manufacturing
2. Suspension bridge cables
3. Aircraft and marine navigation systems that incorporate wind information
4. Express elevators in buildings
5. Library reserve desk
6. Increasing the gate area on a CMOS transistor to decrease its switching time
7. Adding electromagnetic aircraft catapults (which are electrically-powered as opposed to current steam-powered models), allowed by the increased power generation offered by the new reactor technology
8. Building self-driving cars whose control systems partially rely on existing sensor systems already installed into the base vehicle, such as lane departure systems and smart cruise control systems

**1.5**[4] <§1.6> Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

1. Which processor has the highest performance expressed in instructions per second?
2. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

**1.6**[20] <§1.6> Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

1. What is the global CPI for each implementation?
2. Find the clock cycles required in both cases.